

PL4009

N-Channel Enhancement Mode Field Effect Transistor

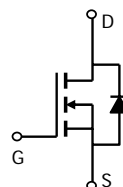
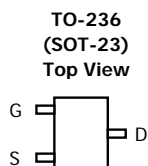


General Description

The PL4009 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a load switch or in PWM applications. *Standard Product PL4009 is Pb-free (meets ROHS & Sony 259 specifications). PL4009A is a Green Product ordering option. PL4009 and PL4009A are electrically identical.*

Features

V_{DS} (V) = 30V
 I_D = 5.8 A (V_{GS} = 10V)
 $R_{DS(ON)} < 28m\Omega$ (V_{GS} = 10V)
 $R_{DS(ON)} < 33m\Omega$ (V_{GS} = 4.5V)
 $R_{DS(ON)} < 52m\Omega$ (V_{GS} = 2.5V)



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 12	V
Continuous Drain Current ^A	I_D	5.8	A
$T_A=25^\circ\text{C}$			
Current ^A	$T_A=70^\circ\text{C}$	4.9	
Pulsed Drain Current ^B	I_{DM}	30	
Power Dissipation ^A	$T_A=25^\circ\text{C}$	1.4	W
	$T_A=70^\circ\text{C}$	1	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$t \leq 10s$	$R_{\theta JA}$	65	90	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^A	Steady-State		85	125	$^\circ\text{C/W}$
Maximum Junction-to-Lead ^C	Steady-State	$R_{\theta JL}$	43	60	$^\circ\text{C/W}$



Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =24V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±12V			100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	0.7	1.1	1.4	V
I _{D(ON)}	On state drain current	V _{GS} =4.5V, V _{DS} =5V	30			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =5.8A T _J =125°C		22.8 32	28 39	mΩ
		V _{GS} =4.5V, I _D =5A		27.3	33	mΩ
		V _{GS} =2.5V, I _D =4A		43.3	52	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =5A	10	15		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.71	1	V
I _S	Maximum Body-Diode Continuous Current				2.5	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =15V, f=1MHz		823	1030	pF
C _{oss}	Output Capacitance			99		pF
C _{rss}	Reverse Transfer Capacitance			77		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		1.2	3.6	Ω
SWITCHING PARAMETERS						
Q _g	Total Gate Charge	V _{GS} =4.5V, V _{DS} =15V, I _D =5.8A		9.7	12	nC
Q _{gs}	Gate Source Charge			1.6		nC
Q _{gd}	Gate Drain Charge			3.1		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =15V, R _L =2.7Ω, R _{GEN} =3Ω		3.3	5	ns
t _r	Turn-On Rise Time			4.8	7	ns
t _{D(off)}	Turn-Off DelayTime			26.3	40	ns
t _f	Turn-Off Fall Time			4.1	6	ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =5A, dI/dt=100A/μs		16	20	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =5A, dI/dt=100A/μs		8.9	12	nC

A: The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design. The current rating is based on the ≤ 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C: The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

D: The static characteristics in Figures 1 to 6,12,14 are obtained using 80μs pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

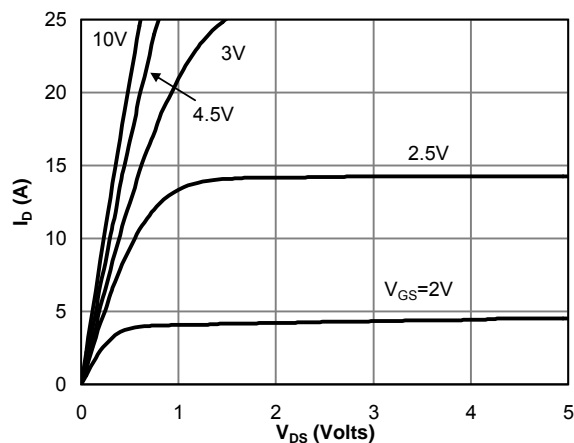


Fig 1: On-Region Characteristics

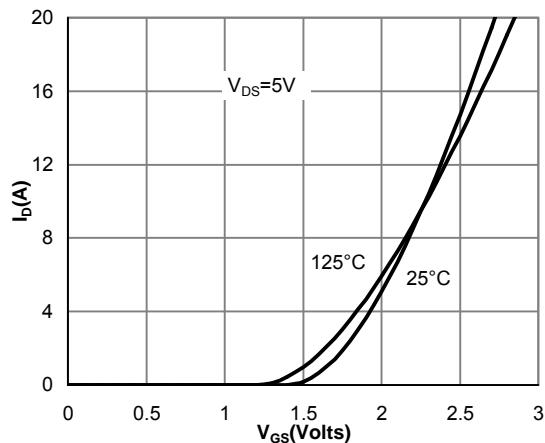


Figure 2: Transfer Characteristics

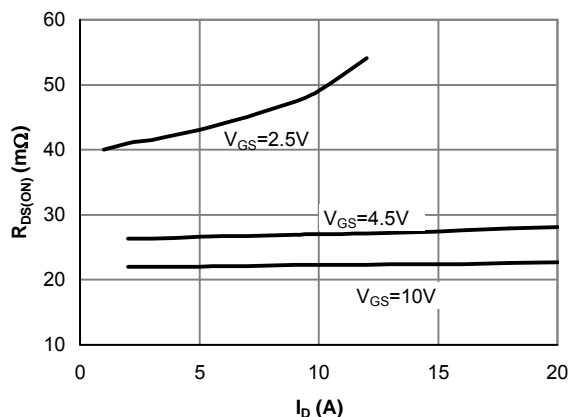


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

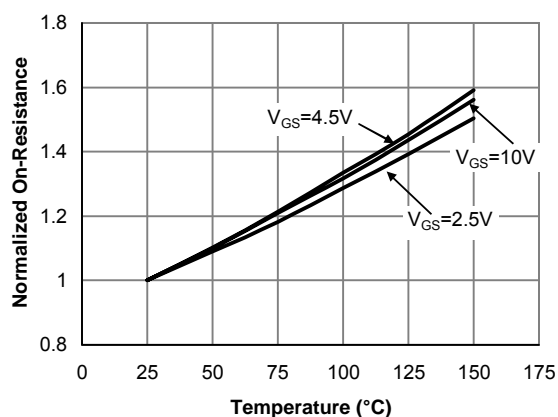


Figure 4: On-Resistance vs. Junction Temperature

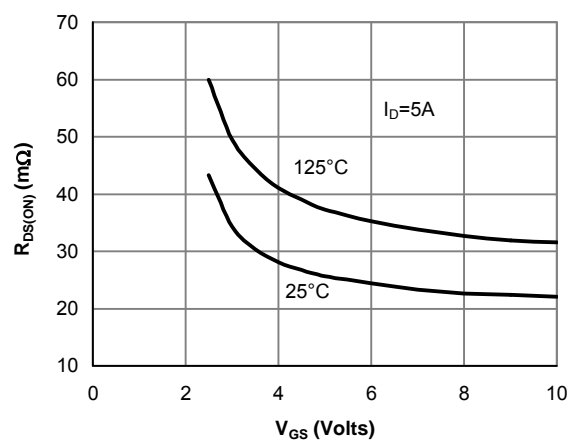


Figure 5: On-Resistance vs. Gate-Source Voltage

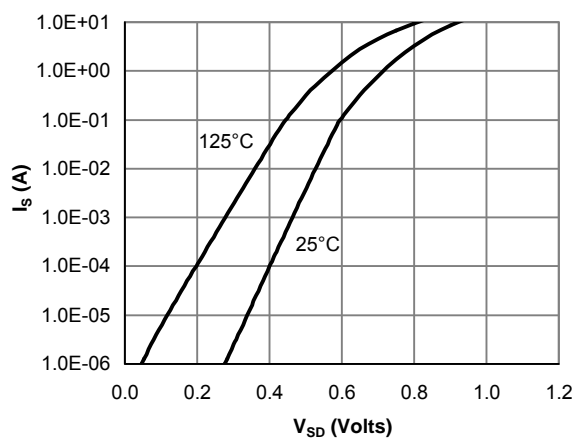


Figure 6: Body-Diode Characteristics



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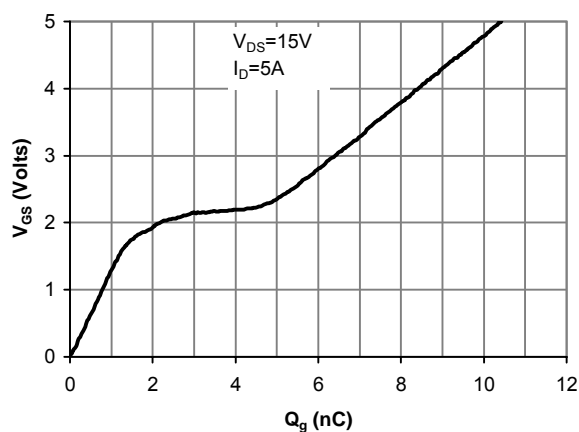


Figure 7: Gate-Charge Characteristics

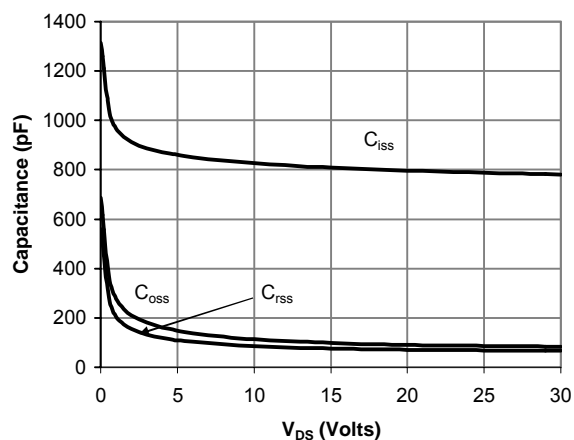


Figure 8: Capacitance Characteristics

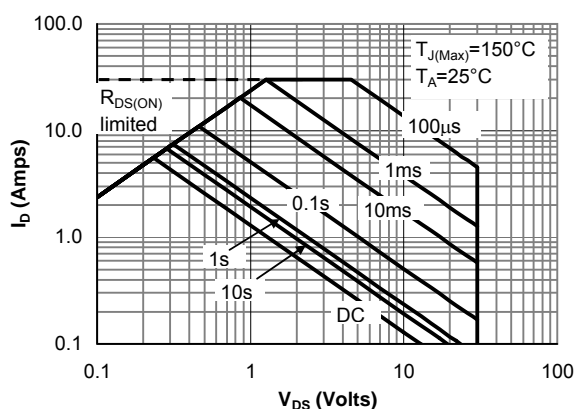


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

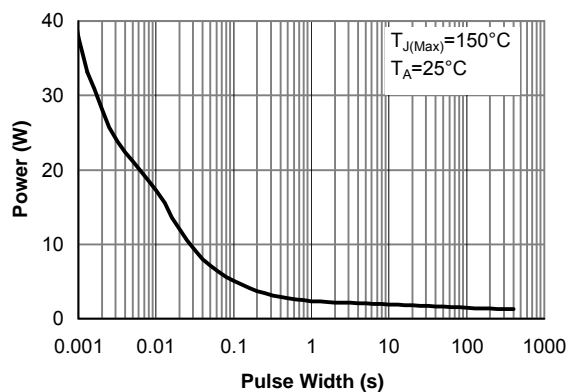


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

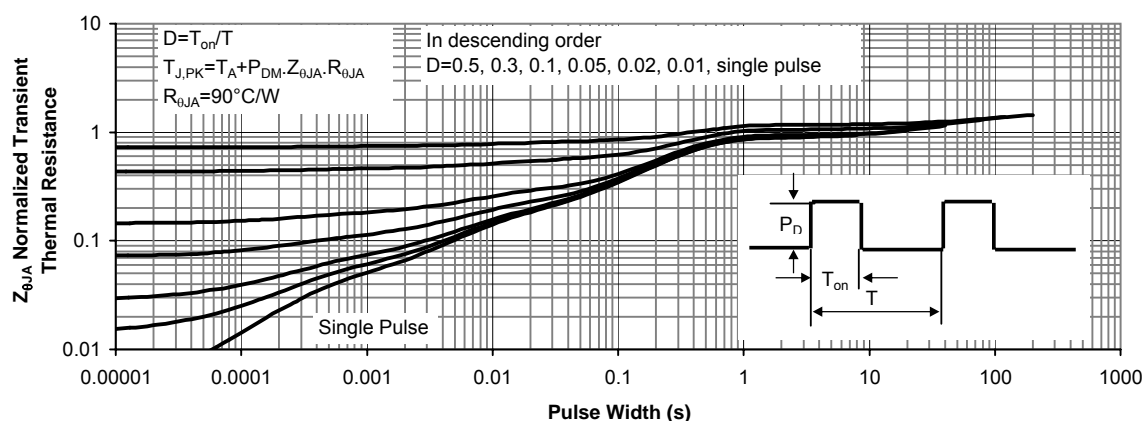


Figure 11: Normalized Maximum Transient Thermal Impedance